ABSTRACT

There is provided a level shifter in which short circuit current and the increase in delay are reduced when a firth power source is controlled.

In a level shifter for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, the circuit has a configuration characterized by including a switching circuit between a GND power source terminal of a level shift core circuit and a GND power source, the switching circuit being controlled by a third logic circuit which generates a control signal under control of the first power source, and a pull-up/pull-down circuit at an output of the level shift core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit.